

Phase-locked loop

NE/SE564

DESCRIPTION

The NE/SE564 is a versatile, high guaranteed frequency phase-locked loop designed for operation up to 50MHz. As shown in the Block Diagram, the NE/SE564 consists of a VCO, limiter, phase comparator, and post detection processor.

FEATURES

- Operation with single 5V supply
- TTL-compatible inputs and outputs
- Guaranteed operation to 50MHz
- External loop gain control
- Reduced carrier feedthrough
- No elaborate filtering needed in FSK applications
- Can be used as a modulator
- Variable loop gain (externally controlled)

APPLICATIONS

- High speed modems
- FSK receivers and transmitters
- Frequency Synthesizers

PIN CONFIGURATIONS

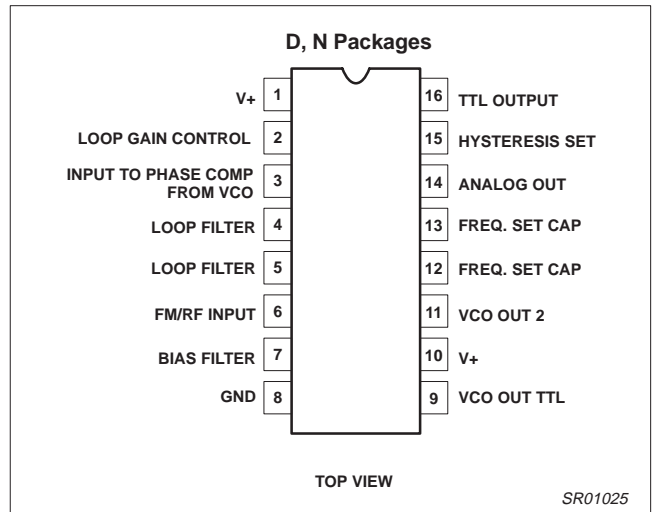


Figure 1. Pin Configuration

- Signal generators
- Various satcom/TV systems
- pin configuration

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
16-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE564D	SOT109-1
16-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE564N	SOT38-4
16-Pin Plastic Dual In-Line Package (DIP)	-55 to +125°C	SE564N	SOT38-4

BLOCK DIAGRAM

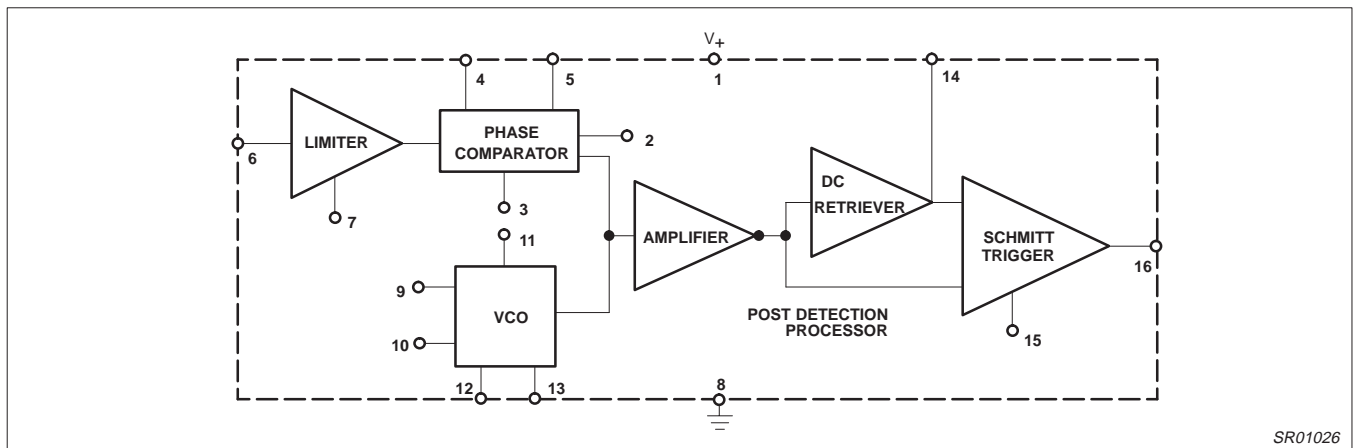


Figure 2. Block Diagram

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V+	Supply voltage Pin 1 Pin 10	14 6	V V
I _{OUT}	Sink Max (Pin 9) and sourcing (Pin 11)	11	mA
I _{BIAS}	Bias current adjust pin (sinking)	1	mA
P _D	Power dissipation	600	mW
T _A	Operating ambient temperature NE	0 to +70	°C
	SE	-55 to +125	°C
T _{STG}	Storage temperature range	-65 to +150	°C

NOTE:

Operation above 5V will require heatsinking of the case.

DC AND AC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V; T_A = 0 to 25°C; f_O = 5MHz, I₂ = 400µA; unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			LIMITS			UNITS
			SE564			NE564			
			MIN	TYP	MAX	MIN	TYP	MAX	
	Maximum VCO frequency	C ₁ = 0 (stray)	50	65		45	60		MHz
	Lock range	Input ≥ 200mV _{RMS} T _A = 25°C T _A = 125°C T _A = -55°C T _A = 0°C T _A = 70°C	40 20 50	70 30 80		40	70 70 40		% of f _O
	Capture range	Input ≥ 200mV _{RMS} , R ₂ = 27Ω	20	30		20	30		% of f _O
	VCO frequency drift with temperature	f _O = 5MHz, T _A = -55°C to +125°C T _A = 0 to +70°C = 0 to +70°C f _O = 5MHz, T _A = -55°C to +125°C T _A = 0 to +70°C		500 300	1500 800		600 500		PPM/°C
	VCO free-running frequency	C ₁ = 91pF R _C = 100Ω "Internal"	4	5	6	3.5	5	6.5	MHz
	VCO frequency change with supply voltage	V _{CC} = 4.5V to 5.5V		3	8		3	8	% of f _O
	Demodulated output voltage	Modulation frequency: 1kHz f _O = 5MHz, input deviation: 2%T = 25°C 1%T = 25°C 1%T = 0°C 1%T = -55°C 1%T = 70°C 1%T = 125°C	16 8 6 12	28 14 10 16		16 8	28 14 13 15		mV _{RMS} mV _{RMS} mV _{RMS} mV _{RMS} mV _{RMS}
	Distortion	Deviation: 1% to 8%		1			1		%
S/N	Signal-to-noise ratio	Std. condition, 1% to 10% dev.		40			40		dB
	AM rejection	Std. condition, 30% AM		35			35		dB
	Demodulated output at operating voltage	Modulation frequency: 1kHz f _O = 5MHz, input deviation: 1% V _{CC} = 4.5V V _{CC} = 5.5V	7 8	12 14		7 8	12 14		mV _{RMS} mV _{RMS}
I _{CC}	Supply current	V _{CC} = 5V I ₁ , I ₁₀		45	60		45	60	mA
	Output "1" output leakage current "0" output voltage	V _{OUT} = 5V, Pins 16, 9 I _{OUT} = 2mA, Pins 16, 9 I _{OUT} = 6mA, Pins 16, 9		1 0.3 0.4	20 0.6 0.8		1 0.3 0.4	20 0.6 0.8	µA V V

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TYPICAL PERFORMANCE CHARACTERISTICS

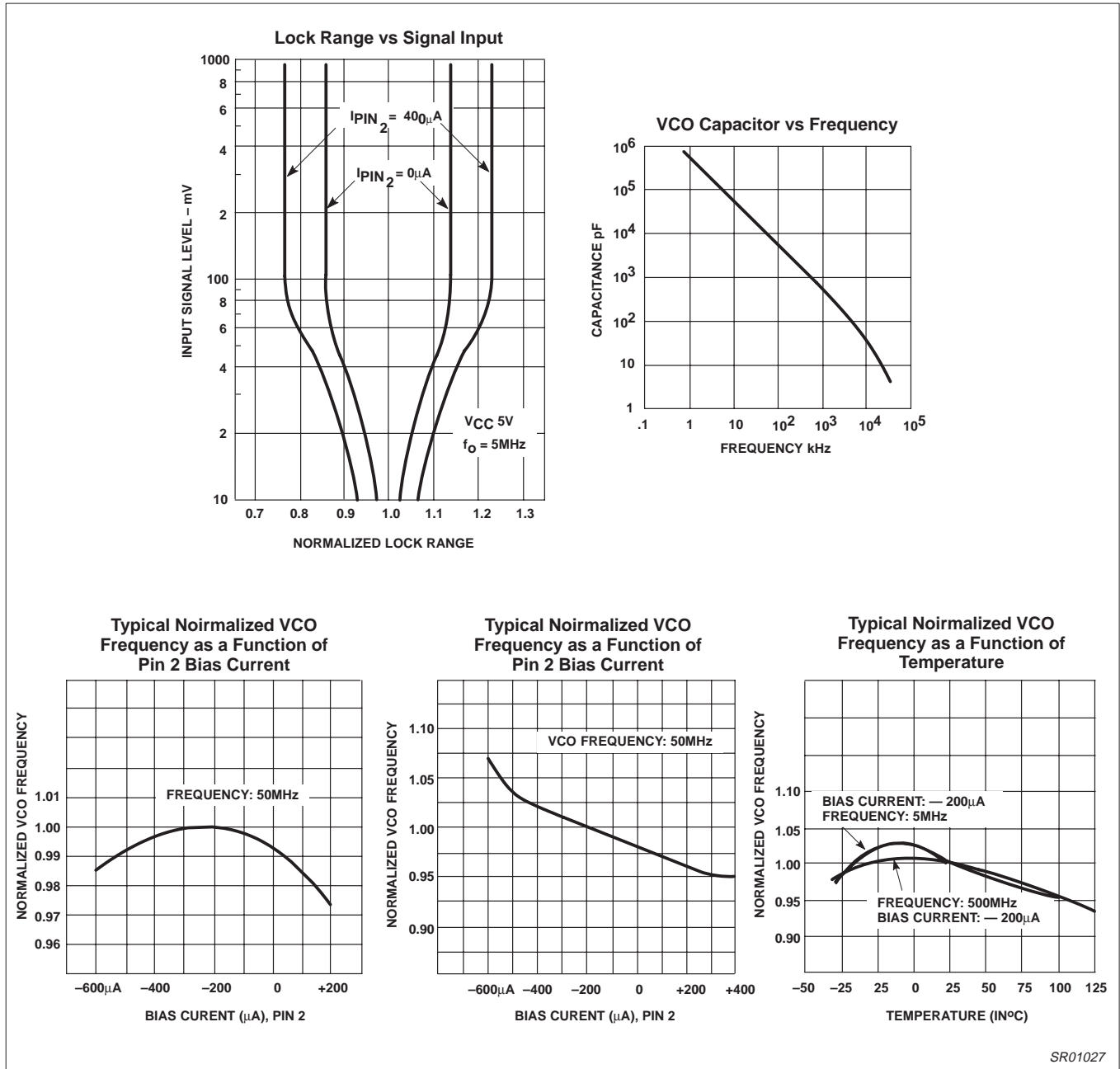


Figure 3. Typical Performance Characteristics

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

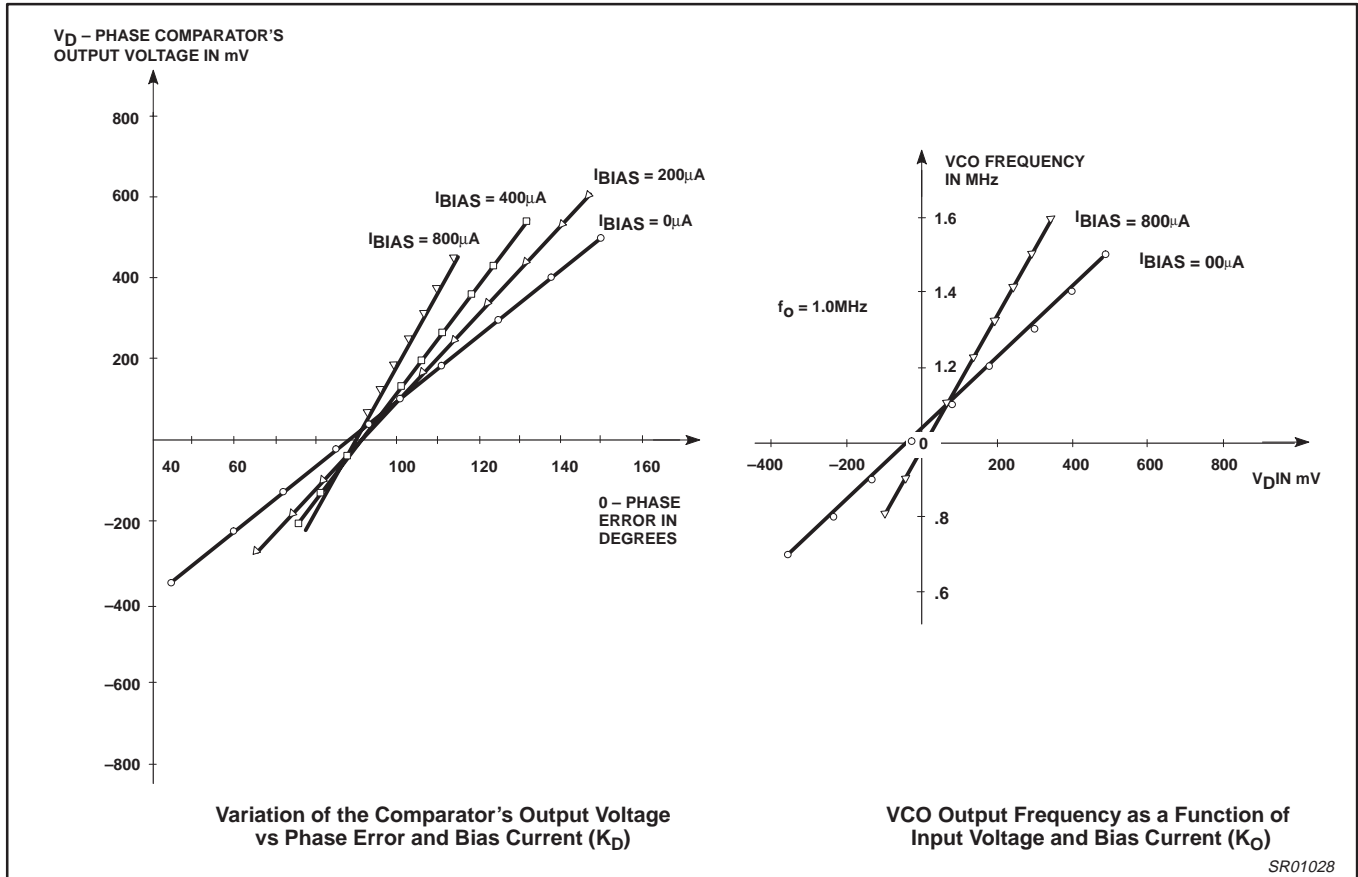


Figure 4. Typical Performance Characteristics (cont.)

TEST CIRCUIT

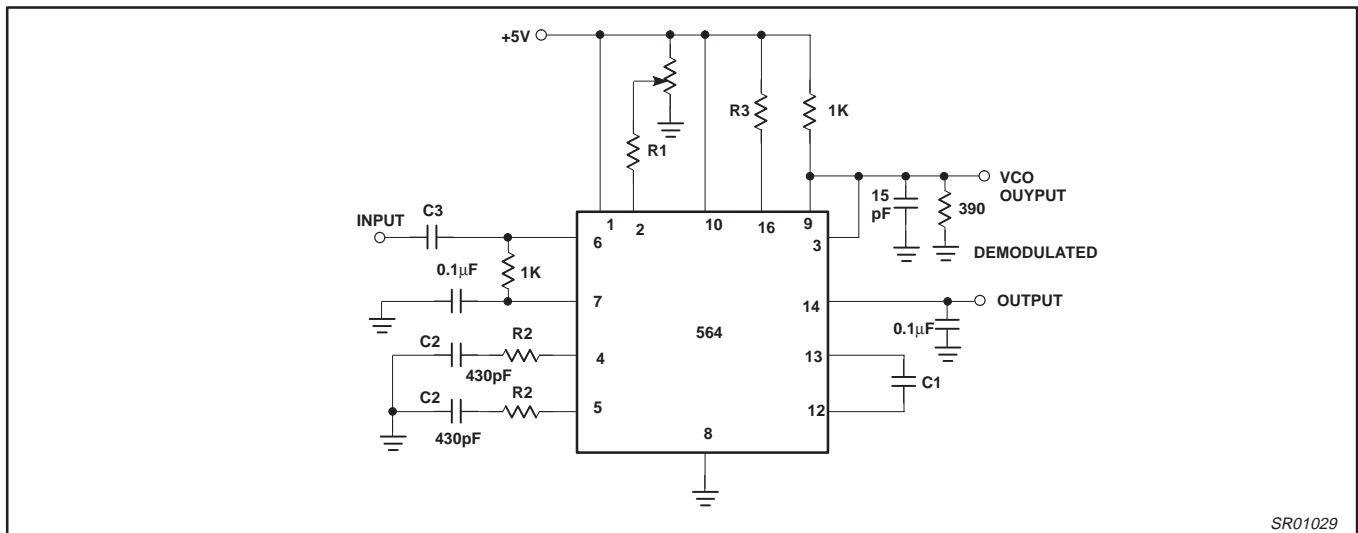


Figure 5. Test Circuit

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FUNCTIONAL DESCRIPTION

(Figure 6)

The NE564 is a monolithic phase-locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50MHz.

In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output of the PLL can be written as shown in the following equation:

$$V_O = \frac{(f_{IN} - f_O)}{K_{VCO}} \quad (1)$$

K_{VCO} = conversion gain of the VCO

f_{IN} = frequency of the input signal

f_O = free-running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by Equation 1 varies according to the frequency deviation of f_{IN} from f_O . Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed, so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at Pin 15 which results in a change of the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature, according to Equation 1 it will lead to a change in the DC levels of the PLL output, and consequently to errors in the digital output signal. This is especially true for narrowband signals where the deviation in f_{IN} itself may be less than the change in f_O due to temperature. This effect can be eliminated if the DC or average value of the signal is retrieved and used as the reference to the comparator. In this manner, variations in the DC levels of the PLL output do not affect the FSK output.

VCO Section

Due to its inherent high-frequency performance, an emitter-coupled oscillator is used in the VCO. In the circuit, shown in the equivalent schematic, transistors Q21 and Q23 with current sources Q25 - Q26 form the basic oscillator. The approximate free-running frequency of the oscillator is shown in the following equation:

$$f_O \cong \frac{1}{22 R_C (C_1 + C_S)} \quad (2)$$

$R_C = R_{19} = R_{20} = 100\Omega$ (INTERNAL)

C_1 = external frequency setting capacitor

C_S = stray capacitance

Variation of V_D (phase detector output voltage) changes the frequency of the oscillator. As indicated by Equation 2, the frequency of the oscillator has a negative temperature coefficient due to the monolithic resistor. To compensate for this, a current I_R with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

Phase Comparator Section

The phase detection processor consists of a doubled-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current in Q_4 and Q_{15} which effectively changes the gain of the differential amplifiers. This can be accomplished by introducing a current at Pin 2.

Post Detection Processor Section

The post detection processor consists of a unity gain transconductance amplifier and comparator. The amplifier can be used as a DC retriever for demodulation of FSK signals, and as a post detection filter for linear FM demodulation. The comparator has adjustable hysteresis so that phase jitter in the output signal can be eliminated.

As shown in the equivalent schematic, the DC retriever is formed by the transconductance amplifier $Q_{42} - Q_{43}$ together with an external capacitor which is connected at the amplifier output (Pin 14). This forms an integrator whose output voltage is shown in the following equation:

$$V_O = \frac{g_M}{C_2} \int V_{IN} dt \quad (3)$$

g_M = transconductance of the amplifier

C_2 = capacitor at the output (Pin 14)

V_{IN} = signal voltage at amplifier input

With proper selection of C_2 , the integrator time constant can be varied so that the output voltage is the DC or average value of the input signal for use in FSK, or as a post detection filter in linear demodulation.

The comparator with hysteresis is made up of $Q_{49} - Q_{50}$ with positive feedback being provided by $Q_{47} - Q_{48}$. The hysteresis is varied by changing the current in Q_{52} with a resulting variation in the loop gain of the comparator. This method of hysteresis control, which is a DC control, provides symmetric variation around the nominal value.

Design Formula

The free-running frequency of the VCO is shown by the following equation:

$$f_O \cong \frac{1}{22 R_C (C_1 + C_S)} \quad (4)$$

$R_C = 100\Omega$

C_1 = external cap in farads

C_S = stray capacitance

The loop filter diagram shown is explained by the following equation:

$$f_S = \frac{1}{1 + sRC_3} \text{ (First Order)} \quad (5)$$

$R = R_{12} = R_{13} = 1.3k\Omega$ (Internal)*

By adding capacitors to Pins 4 and 5, a pole is added to the loop transfer at

$$\omega = \frac{1}{RC_3}$$

NOTE:

*Refer to Figure 6.

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EQUIVALENT SCHEMATIC

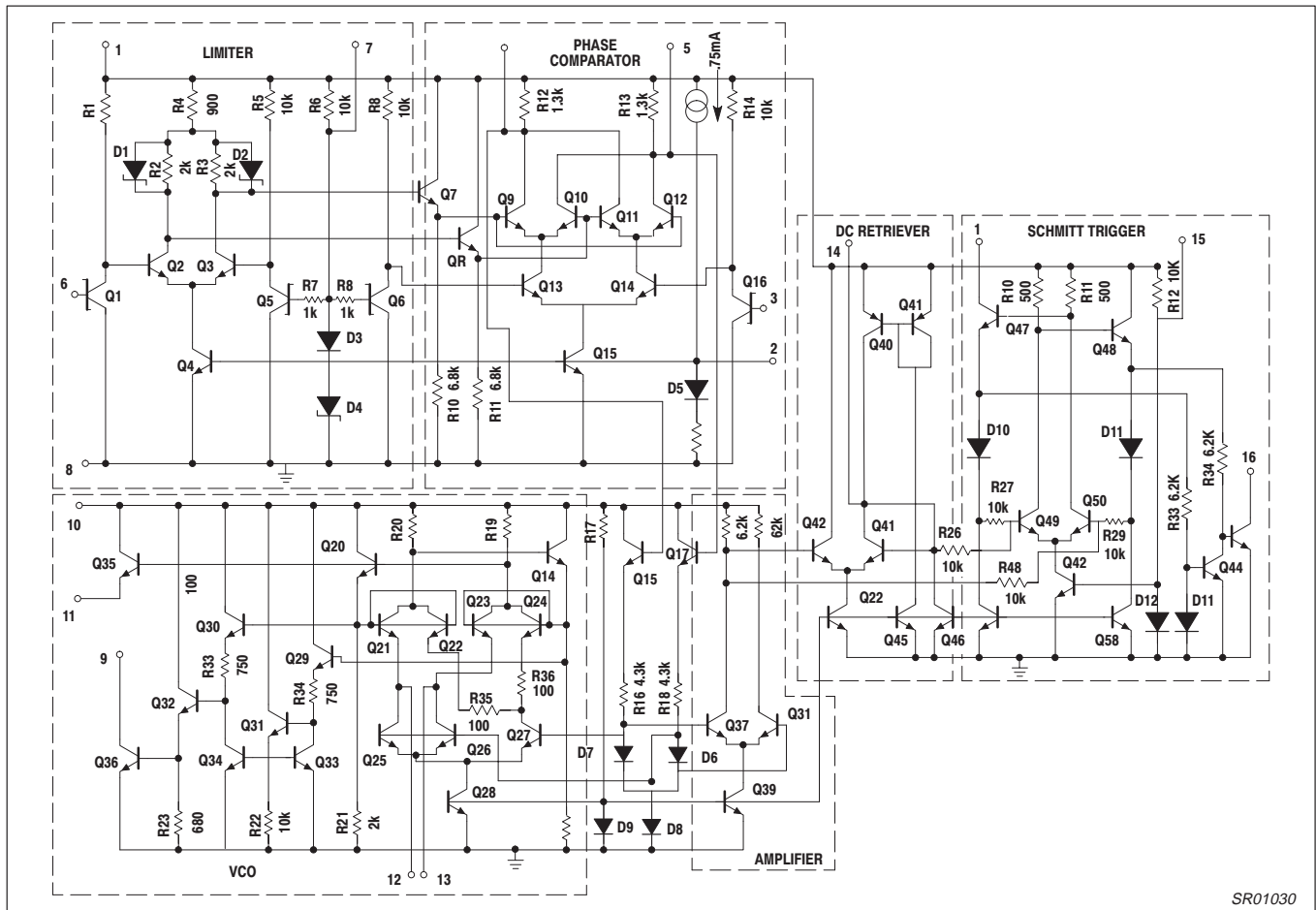


Figure 6. Equivalent Schematic

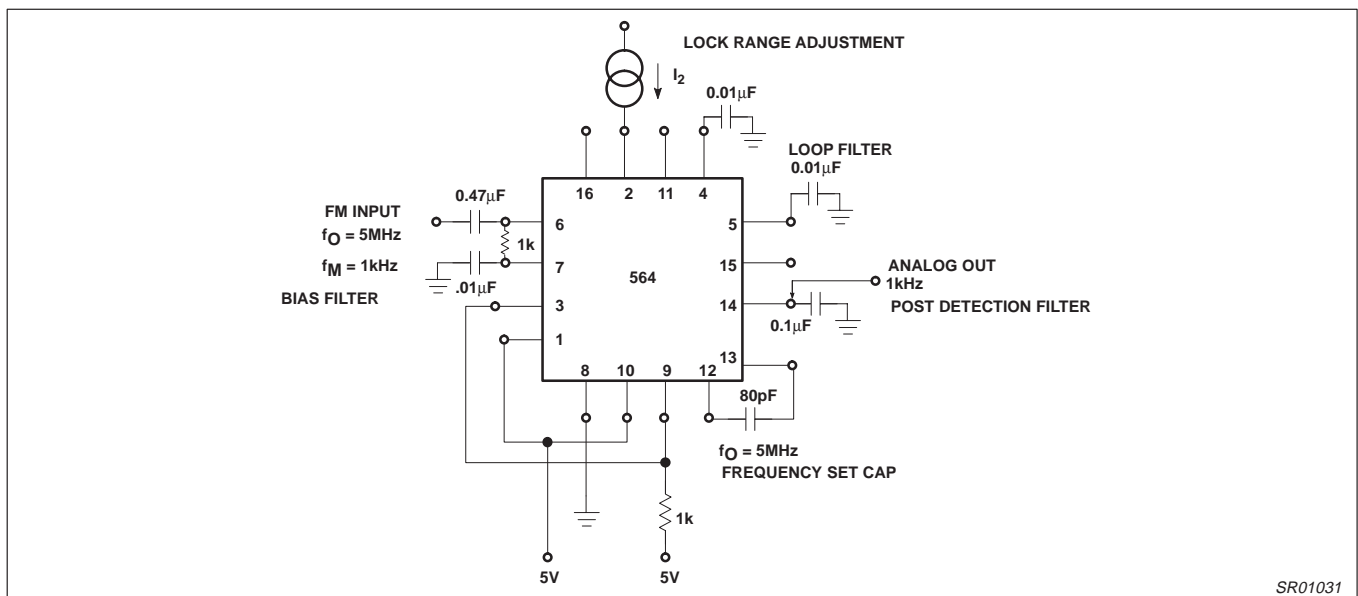


Figure 7. FM Demodulator at 5V

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- 6. If pulsed burst or ramp frequency is used for input signal, special loop filter design may be required in place of simple single capacitor filter on Pins 4 and 5. (See PLL application section)
- 7. The input signal to Pin 6 and the VCO feedback signal to Pin 3 must have a duty cycle of 50% for proper operation of the phase detector. Due to the nature of a balanced mixer if signals are not

- 50% in duty cycle, DC offsets will occur in the loop which tend to create an artificial or biased VCO.
- 8. For multiplier circuits where phase jitter is a problem, loop filter capacitors may be increased to a value of 10 - 50 μ F on Pins 4, 5. Also, careful supply decoupling may be necessary. This includes the counter chain V_{CC} lines.

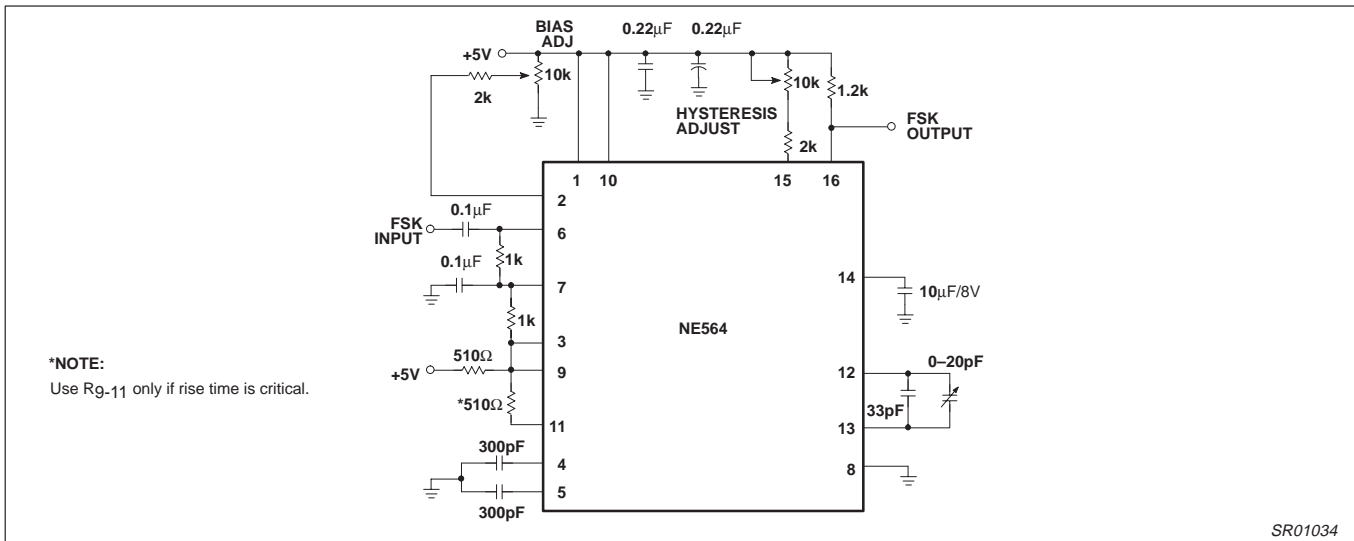


Figure 10. 10.8MHz FSK Decoder Using the 564

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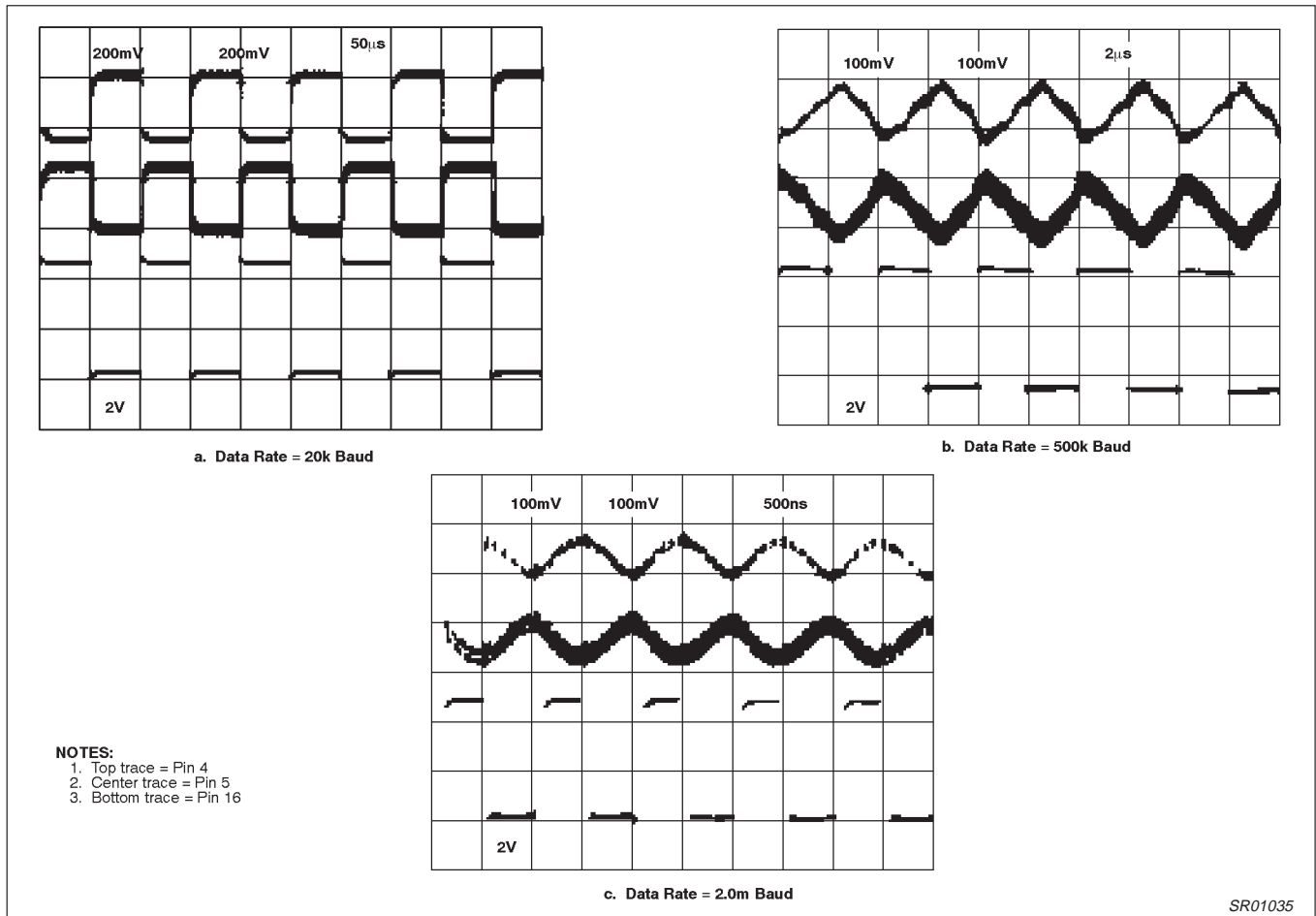


Figure 11. Phase Comparator (Pins 4 and 5) and FSK (Pin 16) Outputs

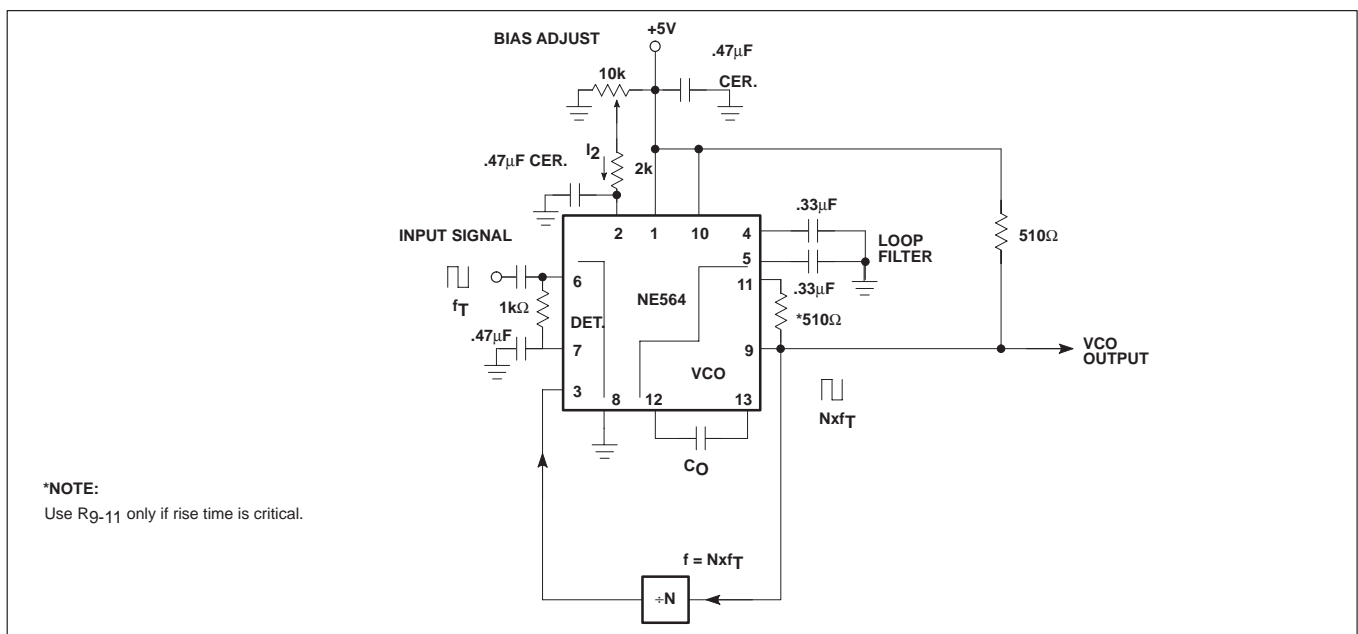


Figure 12. NE564 Phase-Locked Frequency Multiplier